REMARKS

Claims 1-15 and 17-22 were examined and reported in the Office Action. Claims 1-15 and 17-22 are rejected. Claims 4 and 13 are canceled. Claims 1, 5 and 14 are amended. Claims 1-3, 5-12, 14-15 and 17-22 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §103(a)

It is asserted in the Office Action that claims 1-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Application No. 10/750,602 by Lee et al ("Lee"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of

> [a] semiconductor device comprising: a data strobe buffering means for generating N number of align control signals based on a data strobe signal and ~~a~~ an external clock signal; a receiving block in response to N-1 number of the align control signals for

> receiving the plurality of input data and outputting intermediate N-bit data in a parallel fashion; and an outputting block in response to the remaining align control signal for receiving the intermediate N-bit data in the parallel fashion and outputting the intermediate N-bit data in synchronization with the remaining align control signal having an N/2 external clock period to generate the synchronized intermediate N-bit data as the N-bit output data, wherein the semiconductor device operates to receive a plurality of input data to output the N-bit output data at one clock, N being a positive integer, and N is at least 4

Fig. 3 in Applicant's specification illustrates a block diagram of a 4-bit prefetch data input buffer in a conventional synchronous memory device for receiving a plurality of input data to output a 4-bit output data at one clock. In Fig. 3, the semiconductor device includes a data strobe buffering means for generating two align control signals based on a data strobe signal. Applicant's semiconductor device operates to receive a plurality of input data to output the N-bit output data at one clock.

Lee discloses a synchronous 4-bit data sampling circuit having first and second pulse signal generators 31 and 32 for respectively generating two pulse signals. Accordingly, in Applicant's Fig. 3 and Lee, the semiconductor device uses two align control signals for outputting 4-bit output data. Distinguishable, in Applicant's claimed invention, in order to guarantee enough timing margin for a data arranging operation, the data strobe buffering means generates four align control signals corresponding to (the number of) the 4-bit output data. More particularly, a receiving block of the semiconductor device outputs intermediate N-bit data in response to (N-1) the number of the align control signals; and an outputting block outputs the intermediate N-bit data as the N-bit output data in response to the remaining align control signal.

Neither Applicant's admitted prior art nor Lee teach, disclose or suggest the data strobe buffering means for generating N number of align control signals corresponding to the number of the N-bit output data so as to guarantee enough timing margin for a data arranging operation. That is, neither Applicant's admitted prior art nor Lee teach, disclose or suggest "semiconductor device operates to receive a plurality of input data to output the N-bit output data at one clock."

Lee does not teach, disclose or suggest all the limitations of Applicant's amended claim 1, as listed above, Applicant's amended claim 1 is not obvious over Lee since a *prima facie* case of

obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 2-3, 5-12, 14-15 and 17-22, would also not be obvious over Lee for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 1-15 and 17-22 (claim 16 being canceled) is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-3, 5-12, 14-15 and 17-22, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: August 23, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on August 23, 2006.

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Jean Svoboda